



## **UNIQUE CHIP PAIR SIMPLIFIES ISOLATED HIGH SIDE SWITCH DRIVE**

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### *Abstract*

*High voltage, high current N-channel MOSFETs, now widely accepted in the industry, have found their way into numerous high power designs. As their cost to performance ratio continually improves, gate drive circuitry becomes a more significant factor in overall switch cost. This is most notable in "high-side" switching applications where an isolated gate drive is required. A new integrated circuit pair, the UC3724/UC3725, will be presented which implements a simple, isolated MOSFET gate drive circuit. To achieve a cost effective high side switch drive, UNITRODE has developed a unique modulation technique which transmits both signal and power across a small pulse transformer. This publication supercedes Unitrode Application Note U-124, originally written by C. S. Silva.*

### **INTRODUCTION**

Designers of power drives for PWM motor controls and switching power supplies often face the problem of driving the high-side MOSFET transistor in a high voltage power stage. In many applications, for example, bridge and three phase configurations, there are several of these switch drives to implement, and the level of complexity can be discouraging. From a cost standpoint, it is advantageous to utilize N- channel MOSFET devices in comparison to their more expensive - yet easier to drive P- channel counterparts. However, these high-side switch gate drive circuits can quickly become extravagant, and frequently result in complicated or unreliable schemes.

Probably the most common technique used in high-side drive circuits is to generate an isolated, or "floating" auxiliary supply voltage. Referenced to the high-side MOSFET's source, this supply powers a conventional gate drive circuit. The average auxiliary power consumed is generally well below one watt, and varies with switching frequency, FET size and number of paralleled FETs used to configure "one" switch. A typical circuit using this method is shown in figure 1.

With the realization that average MOSFET gate drive power is quite small, charge pump circuits are frequently used to implement the floating supply. In these designs, the storage capacitor can become large in an attempt to minimize the supply's ripple voltage and may impair the useable range of frequencies and duty cycles. Due to this constraint, the switch on-time must be limited by the control circuit, and preferably, under-voltage lockout incorporated in the driver circuit to assure reliable operation.

A simple alternative to this discrete approach can be obtained by using a high voltage IC - provided that the maximum switch voltage and on-time are within it's capability. There is, however, a cost penalty for this single chip solution. While the basic gate drive and protection circuitry have a low voltage requirement, the level shifting transistors necessitate a high voltage IC process - an option which is inherently expensive. Additionally, many motor drive circuits cannot tolerate an on-time limitation, and require an auxiliary power supply for continuous (DC) operation.

Typically, an opto-coupler is used to translate the switch activation command from the ground referenced, or "low-side" control circuitry up to the high-side driver. Unfortunately, this technique comes with its own set of reliability issues which includes low common mode transient immunity, and performance degradation over time and temperature. High voltage MOSFET circuit slew rates

can easily exceed 20 kV/us causing opto-coupler self turn-on or turn-off. The opto-coupler's AC common mode rejection must be carefully evaluated, as this specification is usually influenced by common mode voltage as well as dv/dt. Power up and power down sequences also present potential failure without undervoltage lockout circuitry.

TYPICAL HIGH SIDE DRIVER APPLICATION

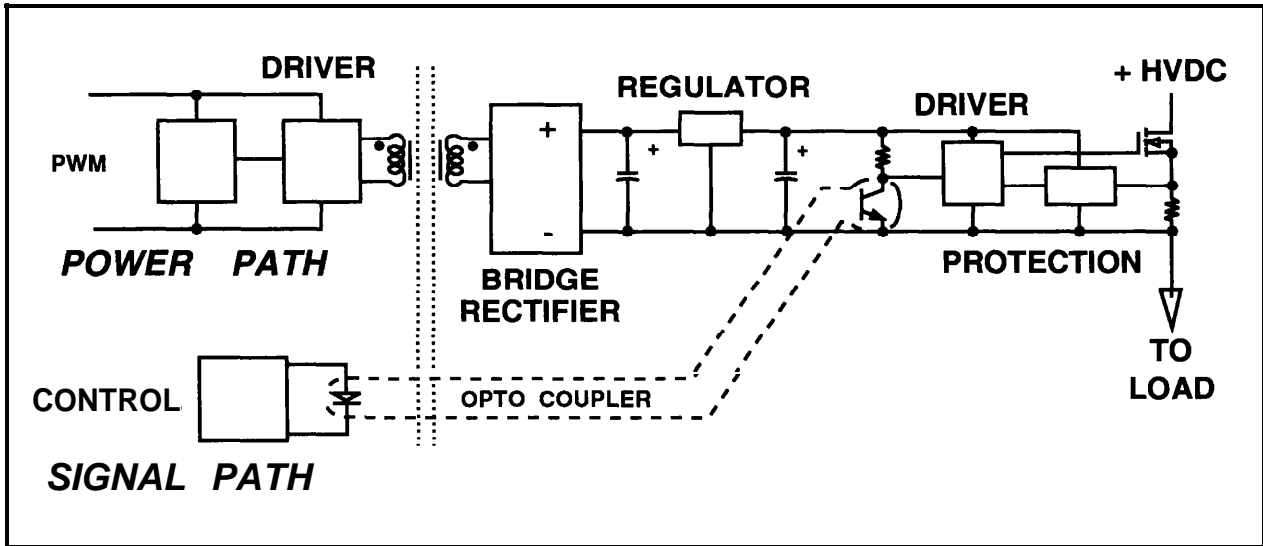


Figure 1.

UC3724 / UC3725 DRIVER PAIR - BASIC CIRCUIT

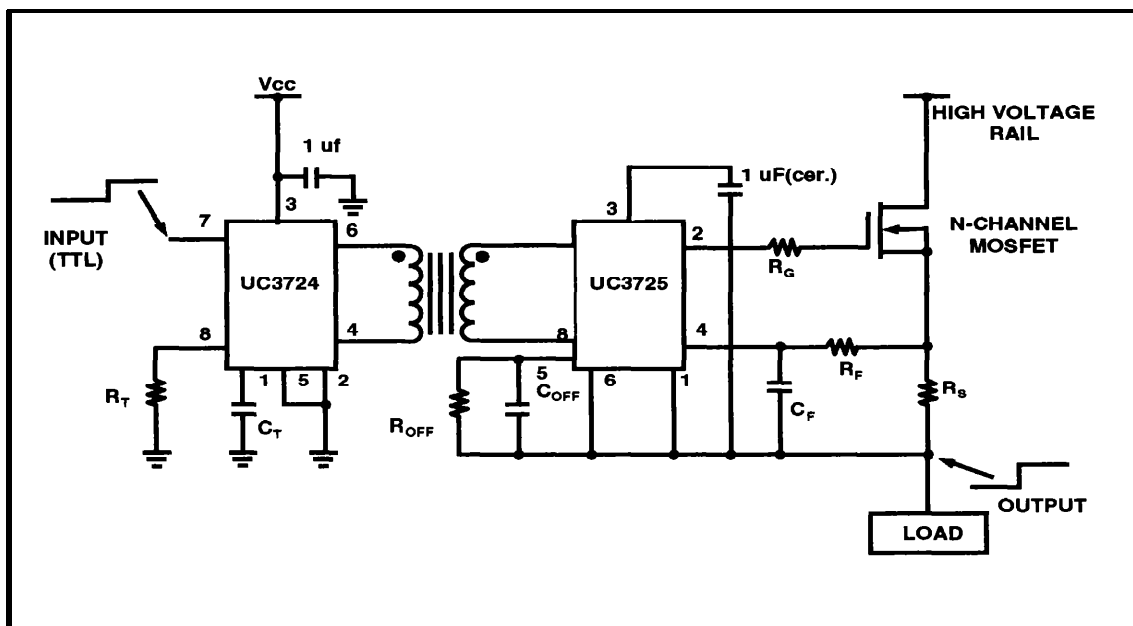


Figure 2.

**UC3724/UC3725 DRIVER PAIR**

The Unitrode UC3724/UC3725 IC pair offers a compact, and comparatively inexpensive design solution to the problem of supplying both isolated power and command signals. Figure 2 shows the basic circuit implementation. The two ICs, a pulse transformer, and a few passive components form a complete isolated MOSFET driver. A unique modulation technique simultaneously transmits power and command information across the transformer.

Provided the operational voltage is low, integrated circuit technology allows sophisticated circuits to be implemented at low cost. Transformers can easily provide several thousand volts of isolation, while supplying both power and signal. By exploiting each device's strengths, a low cost, high performance solution is achieved.

The UC3724 transmitter IC generates the carrier signal, with one of two possible duty cycles as commanded by the TTL level input. A unique carrier oscillator design not only sets the operating frequency, but also prevents the transformer

from saturating, by assuring that the transformer magnetizing current is zero before initiating a subsequent oscillator cycle. Average transformer voltage is always zero, even under the transient conditions caused by input command changes. Saturation of the transformer core is virtually impossible using this technique.

To minimize transformer size and cost, a high frequency carrier is used. Although the carrier frequency limits the maximum transmitted switching frequency, it has no effect on input to output delay, which is solely determined by circuit propagation time.

The UC3725 driver IC rectifies the transformer isolated carrier to power the driver circuitry. Additionally, comparator circuitry determines the input command by sensing which duty cycle is transmitted, driving the MOSFET gate accordingly with the high current output stage. A comparator with programmable off time circuitry implements local over-current protection, while an enable input provides additional control and protection flexibility.

**UC3724 ISOLATED DRIVE TRANSMITTER - BLOCK DIAGRAM**

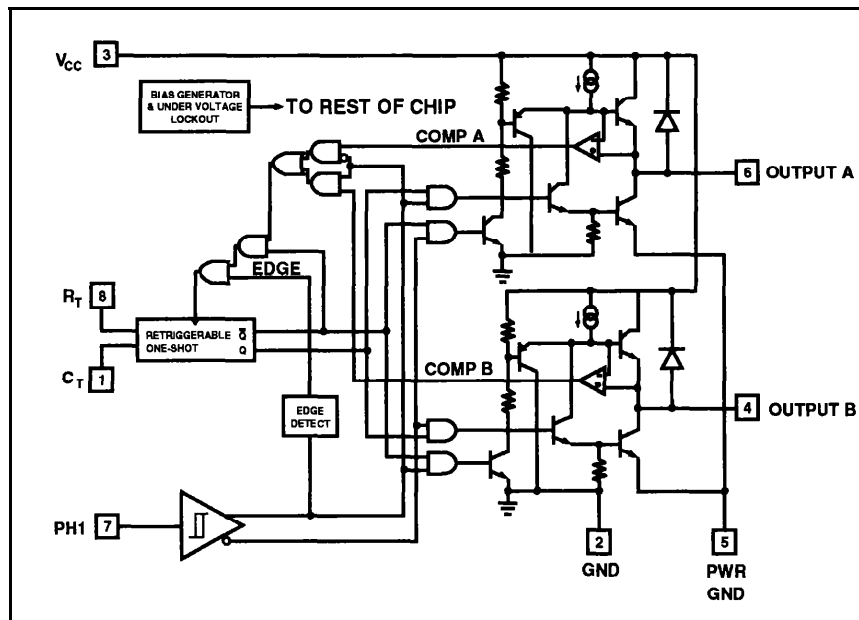


Figure 3.

**UC3724 DRIVE TRANSMITTER**

The UC3724 block diagram is shown in figure 3. The circuit consists of a bias voltage generator with under voltage lockout, control logic, a retriggerable one-shot, a TTL compatible input with hysteresis, two tri-level output drivers, and two

zero current sense comparators.

The under voltage lockout inhibits the output drivers when the input supply voltage is below 9 volts. Once adequate supply voltage is present,

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the bias generator supplies the appropriate internal voltages and currents, allowing the outputs to be enabled. This assures correct operation at power-up and power-down.

The carrier oscillator uses both a one-shot pulse width and the transformer core reset time to set the overall period. The one shot pulse width ( $T_{PW}$ ) equals one-third of the nominal carrier period, and is set by timing resistor ( $R_T$ ) and capacitor ( $C_T$ ).

$$1) T_{PW} = 0.51 \cdot R_T \cdot C_T + 150ns \quad (\text{sec})$$

“Full” supply voltage is applied to the transformer primary during this time by driving one output high and the other low. Transformer magnetizing current rises linearly at a rate determined by the primary inductance and applied voltage.

$$2) di/dt = \frac{V_A - V_B}{L_{pri}} \quad (\text{amps / sec})$$

When the one-shot pulse ends, the low output switches high, and the high output switches to

approximately one-half of the supply voltage. This applies “half” supply voltage to the primary, effectively in a reverse polarity to that of it’s previous state. Internal offset circuitry compensates for output conduction voltage drops and maintains the full/half voltage ratio over temperature and supply voltage variations.

Power is transferred to the secondary circuit only while full voltage is applied to the primary. During this period the primary current is a composite of load and magnetizing current. The load current is interrupted when the half voltage is applied, so the residual primary current flowing is the magnetizing current.

With half voltage applied, the magnetizing current falls at one-half of the rate at which it had increased. An interval twice the programmed one-shot period is therefore necessary to reset the cores magnetizing current to zero and prevent any possibility of core saturation. The UC3724 incorporates a zero current detection circuit which guarantees that the magnetizing current has reached zero before initiating another oscillator cycle.

### UC3724 OPERATIONAL WAVEFORMS (STEADY STATE)

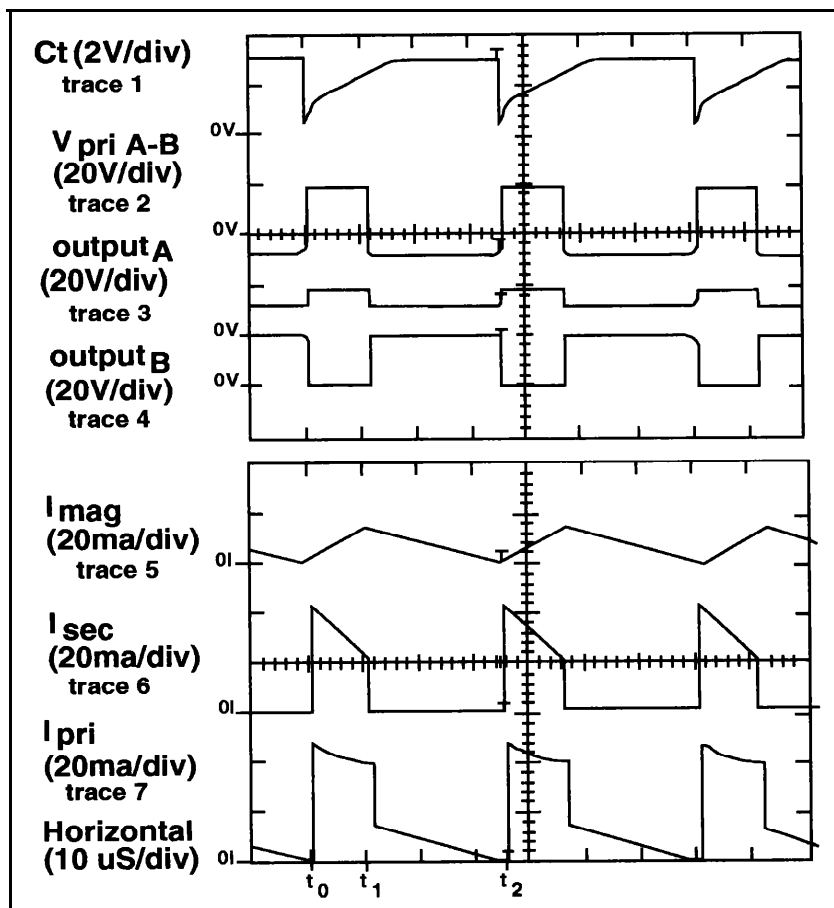


Figure 4.

Steady-state (continuous logic low input command) waveforms are shown in figure 4. The first traceshows timing capacitor ( $C_T$ ) voltage, which is charged by a current set by the timing resistor ( $R_T$ ). At time  $t_0$ , the one-shot is triggered, discharging the timing capacitor. Output<sub>A</sub> (trace 3) switches high, and output<sub>B</sub> (trace 4) switches low, with the resulting differential voltage  $V_{priA-B}$  (trace 2) applied across the transformer primary. The transformer magnetizing current (trace 5) increases linearly at a rate described by equation 2.

At time  $t_1$ , the timing capacitor voltage reaches the 2.5 volt threshold, ending the one-shot period. Output<sub>A</sub> is switched to  $(V_{CC}/2) + V_{offset}$ , and output<sub>B</sub> is switched high, allowing it's catch diode to conduct. The primary voltage ( $V_{priA-B}$ ), is inverted, and reduced in half, causing the magnetizing current to fall at half the rate at which it had increased.

Output<sub>A</sub>'s current sense comparator senses that the magnetizing current has reached zero at  $t_2$  triggering the one-shot, thus initiating another oscillator cycle. If a continuous high is commanded, the waveforms for output<sub>A</sub> and output<sub>B</sub> are interchanged, and the magnetizing current is inverted.

At an input command transition, the existing oscillator cycle is terminated, the A and B outputs are reversed, and a new oscillator cycle is initiated. This applies full voltage of the appropriate polarity across the transformer primary for detection by the UC3725. Although the oscillator cycle has been terminated without allowing the core to reset, there is no danger of saturation. By reversing the outputs, the magnetizing current must first cross through zero before rising in the opposite polarity. The peak magnetizing current is actually less than a normal cycle, reducing the fall time, and hence the oscillator period.

UC3725 ISOLATED SIDE MOSFET DRIVER BLOCK DIAGRAM

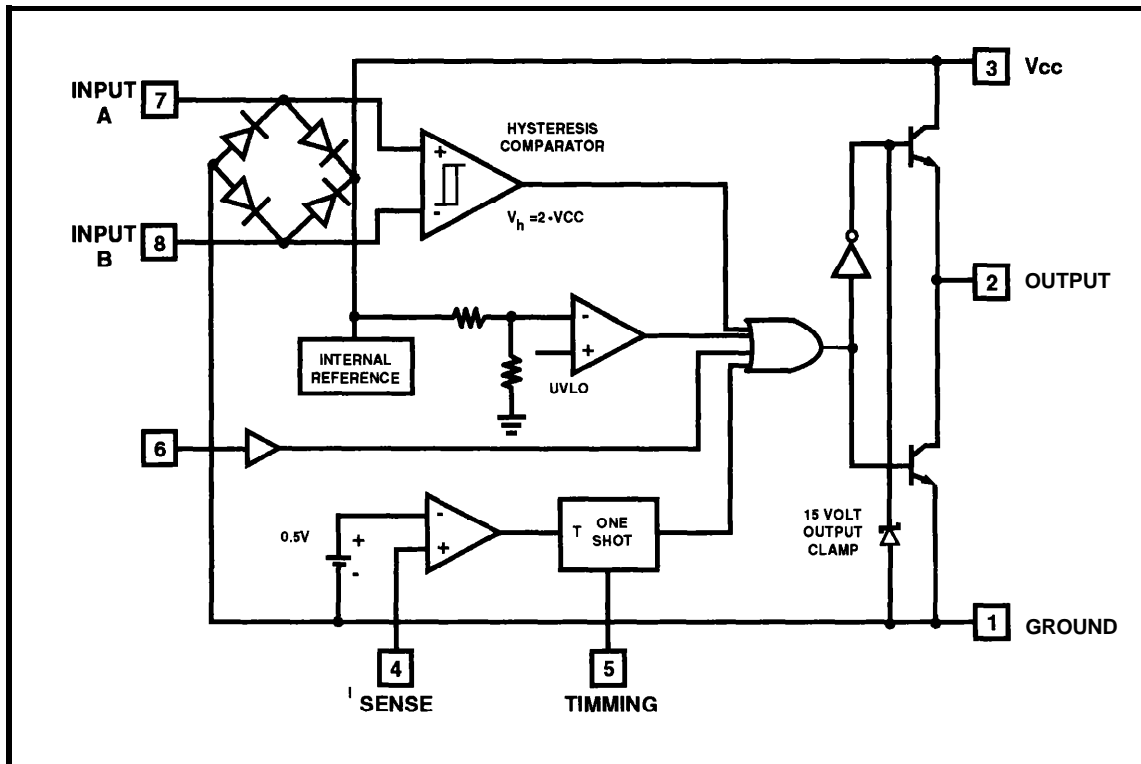


Figure 5.

**UC3725 ISOLATED MOSFET DRIVER**

The block diagram for the UC3725 is shown in figure 5. The circuit consists of a Schottky bridge rectifier, an internal reference with under voltage lock out, a differential hysteresis comparator, a high current totem-pole driver, a current sense comparator with programmable off time one-shot, and an enable input.

The Schottky bridge rectifies the isolated secondary voltage, providing power for the IC. A small capacitor, typically a 1uf ceramic, provides filtering and bulk storage to supply the high peak currents required to rapidly charge the MOSFET gate.

The undervoltage lockout inhibits the output driver when the supply voltage is below 12 volts. This assures that sufficient voltage is available to drive the MOSFET gate, preventing possible destructive linear operation.

The output driver is capable of delivering nearly two amps peak, which is more than adequate for most applications. The UC3725 features a self biasing drive arrangement which actively sinks gate current during under voltage lockout, preventing MOSFET self turn on. No additional gate to source resistor is required. The output voltage is clamped to 15 volts, which along with undervoltage lockout, virtually eliminates the possibility of incorrect gate drive voltages

Over-current protection is provided by monitoring the voltage across a source resistor. The current sense comparator triggers a one-shot, which turns off the MOSFET, when the voltage exceeds 0.5 volts. At power-up,  $C_{off}$  is charged to 7 volts. When an over-current is detected, the output is latched off, and the 7 volt source is disabled allowing  $R_{off}$  to discharge  $C_{off}$ . When  $C_{off}$  discharges to 2 volts, the output is enabled and  $C_{off}$  is charged back to 7 volts. Off time is typically selected to maintain safe MOSFET junction temperature with a continuous fault load, and is programmed by timing resistor ( $R_{off}$ ) and capacitor ( $C_{off}$ ) with the following equation.

$$3) T_{off} = 1.28 \cdot R_{off} \cdot C_{off} \quad (\text{seconds})$$

An enable input allows direct output control for specialized applications. It can be used with level

shifting transistors, optocouplers, or other source referenced circuitry such as a UC3730 thermal monitor circuit for MOSFET over-temperature protection.

The input command, transmitted by the UC3724, is demodulated using a differential hysteresis comparator. The comparator senses whether the "full voltage" applied to the transformer is positive or negative, corresponding to an "off" or "on" input command. The bridge rectifier causes the peak secondary voltage to always be two diode drops above  $V_{cc}$  while the comparator hysteresis is internally set to twice  $V_{cc}$ . The MOSFET is turned on when the secondary voltage is more negative than  $-(V_{cc})$ , and turned off when more positive than  $V_{cc}$ . Note that there is a logic inversion between the hysteresis comparator and the gate driver.

Referring to steady-state waveforms (figure 4) the secondary current (trace 6) charges the supply capacitor during the full voltage output segment of the oscillator cycle (time  $t_0$  thru  $t_1$ ). During the half voltage output segment (time  $t_1$  thru  $t_2$ ), no secondary current flows, thus only magnetizing current is present in the primary current (trace 7) allowing proper oscillator operation.

For this example, a 30% duty cycle input command was arbitrarily selected, and the associated waveforms are shown in figure 6. At time  $t_0$ , the input command (trace 1) transitions from low to high, immediately switching output, low, output, high, and retriggering the one-shot. The differential hysteresis comparator switches low, driving the output (trace 4) high, when the transformer secondary voltage ( $V_{sec A-B}$ , trace 3), is more negative than  $-(V_{cc})$ . The primary current (trace 2) is inverted from the output and output reversal, but power delivery to the IC is unaffected due to the bridge rectifier input.

The input command transitions low at time  $t_1$ , switching output, high, output, low, and retriggering the one-shot. The hysteresis comparator switches high, driving the output low, when the secondary voltage exceeds  $V_{cc}$ . Note the reduced magnetizing current fall time, and associated oscillator period reduction, after input command transitions.

OPERATIONAL WAVEFORMS AT 30% DUTY CYCLE

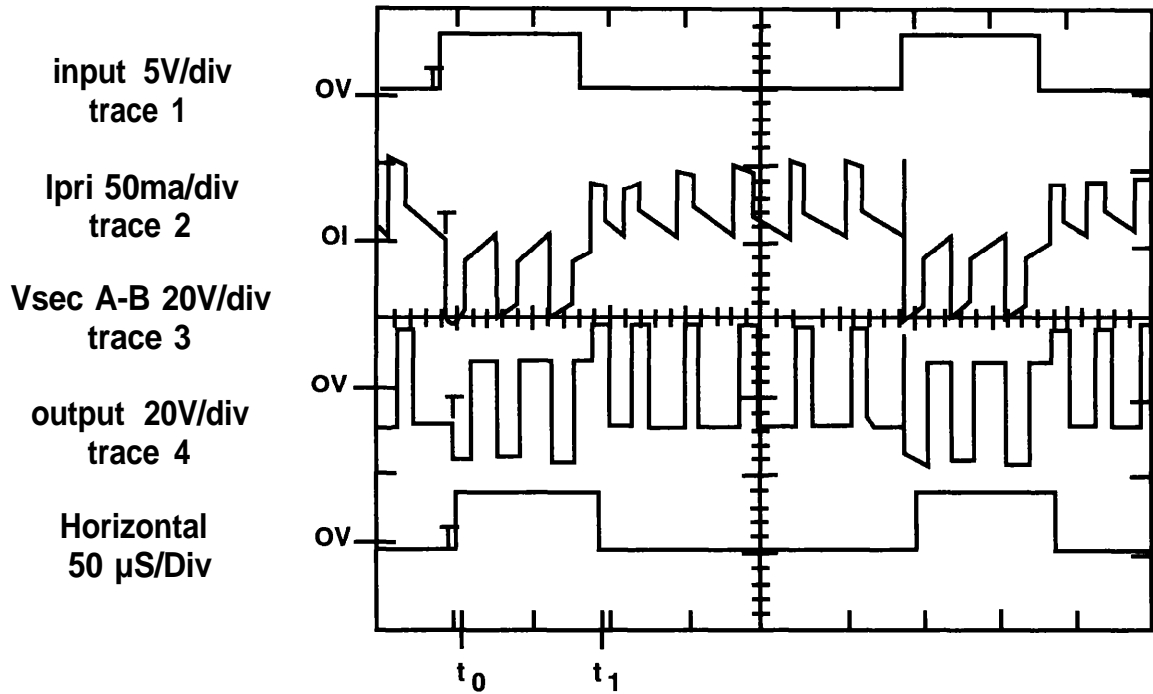


Figure 6.

PRACTICAL CONSIDERATIONS

The selection of carrier frequency (or more appropriately one-shot period since carrier frequency varies at switching transitions), is influenced more by transformer design than performance objectives. The minimum switching command period should be limited to four times the one-shot pulse width, to assure that adequate time is available to reset the core. Note that this limits the maximum switching frequency - but not the duty cycle range which is always 0 to 100%.

Waveforms for a command period approximately four times the one shot pulse width are shown in figure 7. The carrier oscillator has sufficient time to reset the transformer core and prevent saturation.

The one-shot period has no effect on input to output propagation delay, since the leading edge provides the output command information. Turn-on and turn-off propagation delay waveforms are shown in figure 8.

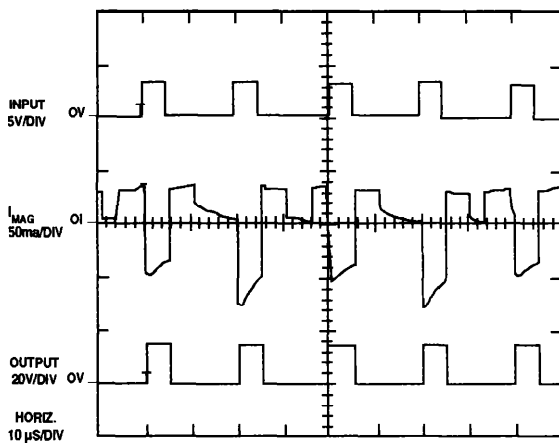


Figure 7.

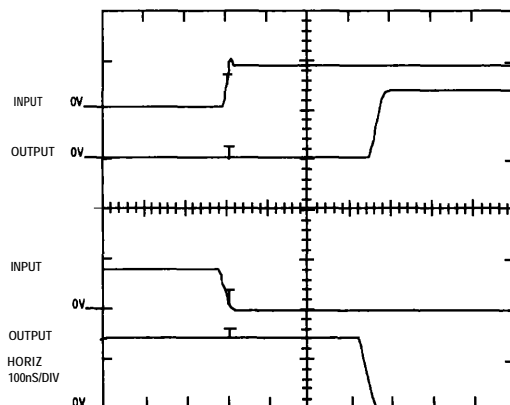


Figure 8.

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The maximum carrier frequency is limited to 600 KHz. Most circuits will operate between 200 and 600 KHz., allowing switching frequencies up to 450 KHz., and a simple low cost transformer design. Nominal carrier frequency is calculated using equation 4.

$$4) F_c = \frac{1}{3 \cdot T_{PW}} \quad (\text{Hz})$$

where  $T_{PW}$  = one-shot pulse width  
from equation 1.

Power supply voltage directly affects dissipation in the transmitter IC. Typical supply current verses voltage for the UC3724 is shown in figure 9. In most applications, bias power loss is about half of the total power dissipation.

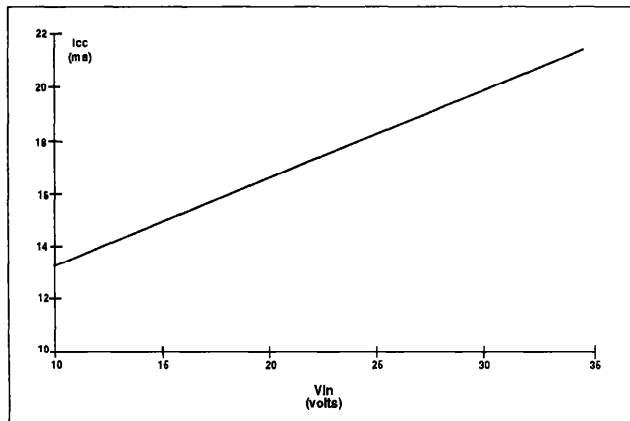


Figure 9.

The UC3725 driver IC provides sufficient gate voltage with a 15volt supply. Any further increase, although safe since the output is clamped to 15 volts, causes additional bias power dissipation. By adjusting the transformer turns ratio, a 15 to 18 volt secondary supply can be generated with any primary voltage, allowing maximum efficiency.

Magnetizing current also contributes towards increasing dissipation with supply voltage. Although the UC3724 outputs can handle several hundred milliamps of load current with the output transistors in saturation, nearly one-half  $V_{cc}$  is across the upper transistors during the magnetizing current fall time. Dissipation during this period usually limits the peak magnetizing current, although catch diode current (which only conducts falling magnetizing current) is limited to 50 mA peak. When the peak magnetizing current falls below 10 ma, the required primary inductance

becomes excessive, resulting in a large number of turns or larger core size. Therefore, the optimal range of peak magnetizing current is between 10 and 40 mA.

In many applications, the average gate charge current delivered by the driver is insignificant in relation to the UC3725 bias current. When larger MOSFETs, particularly large parallel assemblies, are driven at higher frequencies, the average gate charge current will have a considerable effect on the total transformer load. Average gate charge current is the product of gate charge ( $Q_g$ ), which is specified by the MOSFET manufacturer, and the switching frequency.

$$5) I_g (\text{avg.}) = Q_g \cdot F_s \quad (\text{amps})$$

where  $Q_g$  = gate charge  
 $F_s$  = switching frequency

All of the charge delivered to the gate at turn-on must be removed at turn-off. The resultant average power dissipated by the driver and gate resistor is described by equation 6.

$$6) P_g = Q_g \cdot V_g \cdot F_s \quad (\text{Watts})$$

where  $V_g$  = fully charged gate  
voltage

The over-current input on the UC3725 has a typical delay time of 150 ns. Most applications require a small RC filter to attenuate leading edge current spikes caused by parasitic capacitance and catch rectifier reverse recovery. Careful attention to layout and component selection is necessary to prevent false triggering. The current sense resistor should be non-inductive to minimize spiking and ringing. The filter capacitor should be located as close to the IC as possible, with direct connections to the comparator input and common. The connection between the UC3725 common, and the MOSFET source resistor, must have relatively low impedance to prevent gate drive current from affecting current sense accuracy. In addition this should be a "Kelvin" connection, such that no load current flows through it. If the current sense feature is not required, the comparator input is simply connected to common, and the timing input is allowed to float.



## DESIGN PROCEDURE

Typically, the application dictates the MOSFET(s), switching frequency, and switch isolation voltage. For cost considerations, a supply voltage common with other circuitry, is usually chosen to power the UC3724. The designer is then left with the carrier frequency and peak magnetizing current to select. A high carrier frequency is normally used to minimize transformer size and cost. Magnetizing current is initially set to a nominal value, such as 20 ma, and then adjusted if necessary to optimize the transformer design.

The one-shot pulse width is set to 1/3 the carrier frequency using equation 1. By rearranging equation 2, and allowing 2 volts for saturation, the transformer primary inductance can be calculated.

$$7) L_{pri} = \frac{(V_{cc}-2) \cdot T_{pw}}{I_{mag}} \quad (\text{H e n r i e s})$$

where  $V_{cc}$  = supply voltage  
 $T_{pw}$  = one-shot pulse width  
 $I_{mag}$  = peak transformer magnetizing current

Transformer core selection is an iterative process based on the following two equations.

$$8) \Delta B = \frac{V_{applied} \cdot T_{on} \cdot 10^4}{N_{turns} \cdot A_c} \quad (\text{Tesla})$$

$$9) N_{turns} = \sqrt{\frac{L_{pri} \cdot 10^9}{A_L}} \quad (\text{turns})$$

A toroid is usually the most cost effective core geometry for this application. The core material should be chosen for low losses and high permeability at the design frequency to minimize transformer size and number of turns. Thermal resistance and loss factors provided by the manufacturer are used to select the optimum core size. A flux density of .05 Tesla (500 Gauss) will cause approximately a 20 degree C rise at 500 KHz with common power materials such as Ferroxcube 3C8.

Typically most toroids used for this application have an  $A_L$  between 1000 and 3000 mH/1000 turns. An estimated number of turns is calculated using an average  $A_L$  value of 2000 mH/1000 turns in equation 8. By rearranging equation 7, an approximate core are is calculated using a flux density of .05 Tesla, and the estimated number of turns. This leads to a first core selection, and an actual  $A_L$  value, which is used in equation 8 to calculate  $N_{turns}$ . The flux density is then checked using equation 7, and a larger or smaller core is selected if necessary.

The turns ratio is calculated using the following equation, which allows 2 volts for UC3724 output saturation, and 3 volts for UC3725 rectifier drop and output saturation.

$$10) \text{ Turns ratio} = \frac{V_{cc}-2}{V_{gate}+3}$$

The power supplied by the transformer is the sum of the UC3725 bias loss and the average gate charge power. For minimum wire size, the resulting RMS winding currents can be calculated, although typically there sufficient space to use 24 to 28 AWG wire for ease of handling.

High voltage isolation is implemented by sleaving the primary winding with an insulation suitable for the required breakdown voltage. For low leakage inductance, bifilar windings are used, with additional turns added to the primary or secondary for non 1:1 turns ratios.

## DESIGN EXAMPLE

The following design example is a general purpose isolated MOSFET gate driver. Up to 200 milliwatts is available for gate drive, which is suitable for most applications. A 15 volt power supply provides sufficient secondary voltage by using a step-up transformer.

Driver specifications:

- \* 200 milliwatts average gate drive power
- \* 100 KHz. switching rate
- \* 15 V supply voltage
- \* 1KV minimum isolation voltage

A 600KHz. carrier frequency is selected to minimize transformer size and cost. The one-shot pulse width is calculated by rearranging equation 4.

$$T_{pw} = \frac{1}{3 \cdot 600 \text{ KHz}}$$

$$= 556 \text{ ns}$$

Since the carrier frequency is near maximum, 2K will be used for  $R_T$ .  $C_T$  is calculated with equation 1.

$$C_T = \frac{(556-150) \text{ ns}}{0.51 \cdot 2\text{K}}$$

$$= 398 \text{ pf (use 390pf)}$$

30mA is selected for the peak magnetizing current. The corresponding primary inductance is calculated with equation 7.

$$L_{pri} = \frac{(15-2) \text{ V} \cdot 556 \text{ ns}}{30 \text{ mA}}$$

$$= 241 \mu\text{H}$$

The estimated number of turns are calculated using equation 9 with an average value of 2000 mH/1000 turns for  $A_L$ .

$$N_{turns} = \sqrt{\frac{241 \cdot 10^9}{2000}}$$

$$= 11 \text{ turns}$$

The approximate core area is calculated with equation 8, using a flux density of 0.05 Tesla.

$$A_c = \frac{13\text{V} \cdot 556 \text{ ns} \cdot 10^4}{11 \text{ turns} \cdot 0.05 \text{ Tesla}}$$

$$= 0.131 \text{ cm}^2$$

A one-half inch diameter toroid, Ferroxcube part number 204T250-3C8, is selected which has the following specifications.

$$A_c = 0.148 \text{ cm}^2$$

$$A_L = 1620 \text{ mH/1000 turns}$$

$N_{turns}$  is calculated using the actual  $A_c$  value in equation 9.

$$N_{turns} = \sqrt{\frac{241 \cdot 10^9}{1620}}$$

$$= 12.2 \text{ turns (use 12 turns)}$$

The flux density is checked using equation 8.

$$\Delta B = \frac{(15-2) \text{ V} \cdot 556 \text{ ns} \cdot 10^4}{12 \text{ turns} \cdot 0.148 \text{ cm}^2}$$

$$= 0.041 \text{ Tesla}$$

The turns ratio is calculated using equation 10 for a gate voltage of 12 to 14 volts.

$$\text{Turns ratio} = \frac{(15-2) \text{ V}}{(12+3) \text{ V}}$$

$$= 0.867$$

Therefore  $N_{sec} = 14$  turns

The transformer is wound with 26AWG magnet wire for ease of handling. A teflon insulation sleeve is slipped over the primary winding to improve the primary to secondary breakdown voltage. The primary and secondary are wound bifilar, to minimize leakage inductance, then the two remaining secondary turns are wound.

To verify operation, the test circuit shown in figure 10 was built. The over current, gate and bulk storage components are selected per MOSFET and load requirements. Figure 11 and 12 show turn-on and turn-off waveforms respectively.

The lower MOSFET in figure 10 was configured to test self turn-on of the upper driver during high transformer dv/dt. With 300 volts slewing at a rate in excess of 25 kv/us, no evidence of driver self turn-on was observed.

## APPLICATIONS

Although the lower MOSFET driver is configured for faster switching than would normally be required, figure 10 is typical of half bridge outputs, where two or three of these circuits could implement a full or three phase bridge respectively. Full isolation for UL or VDE requirements can be met

by using isolated drivers for both upper and lower MOSFETs. This configuration can also greatly reduce noise in high current applications, by com-

pletely isolating the control circuitry from output devices.

TYPICAL HIGH SIDE DRIVE APPLICATION CIRCUIT SCHEMATIC

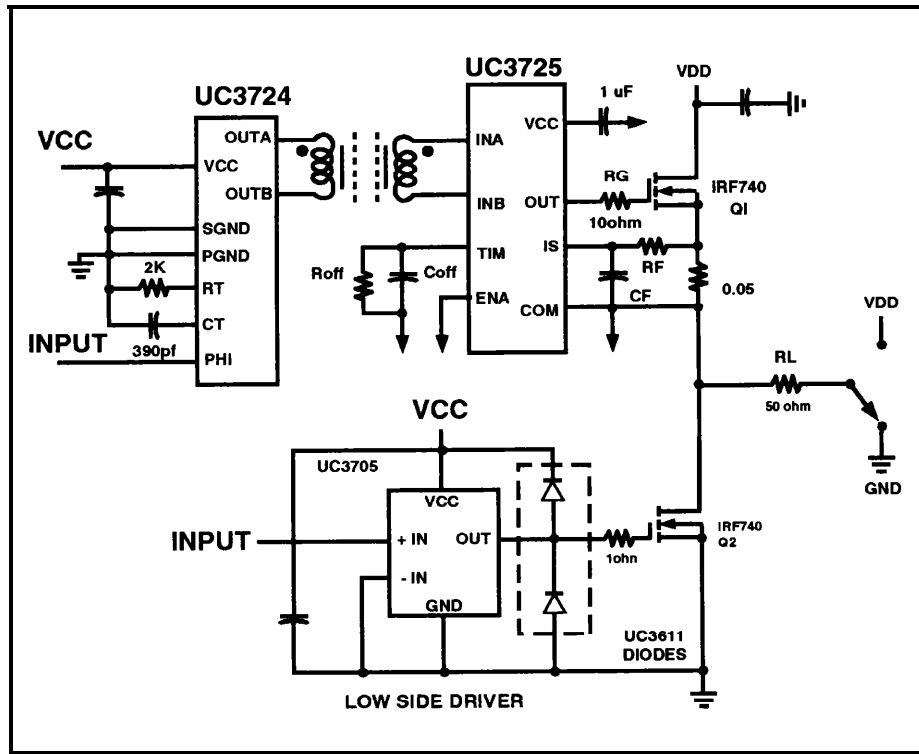


Figure 10

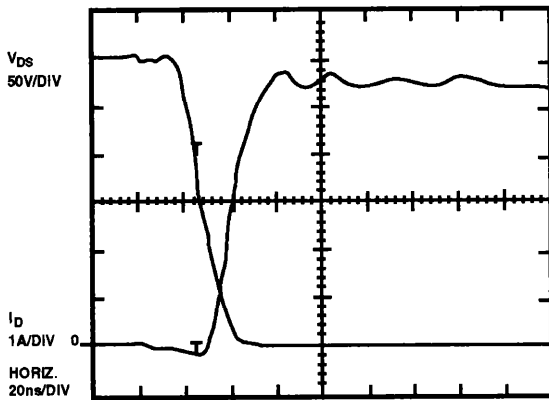


Figure 11

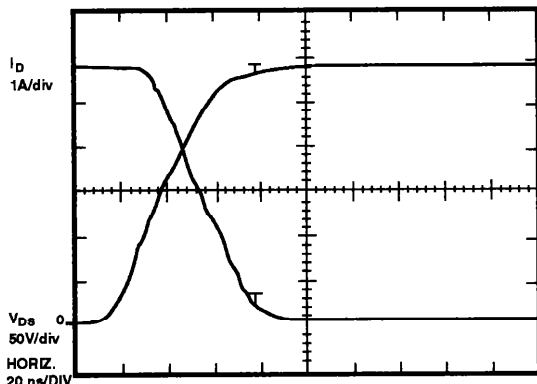


Figure 12

FULL BRIDGE OUTPUT

Some circuits have multiple MOSFETs driven from the same command, which are isolated from each other. A most notable example is the full bridge, which is commonly used in brush and stepper motor drives. Multiple secondaries can drive additional isolated UC3725 circuits, from a single UC3724, further reducing cost and complexity.

Figure 13 shows a fully isolated bridge circuit. By isolating all of the MOSFETs and the current sense signal, complete control to output isolation is achieved. Dual secondaries on each transformer eliminates the requirement for two additional transformers and UC3724s. For feedback and protection, a hall effect current sensor monitors load current directly, while providing high voltage isolation. The local over-current circuit in the upper FET drivers protects during load to ground shorts.

FULL BRIDGE OUTPUT CIRCUIT

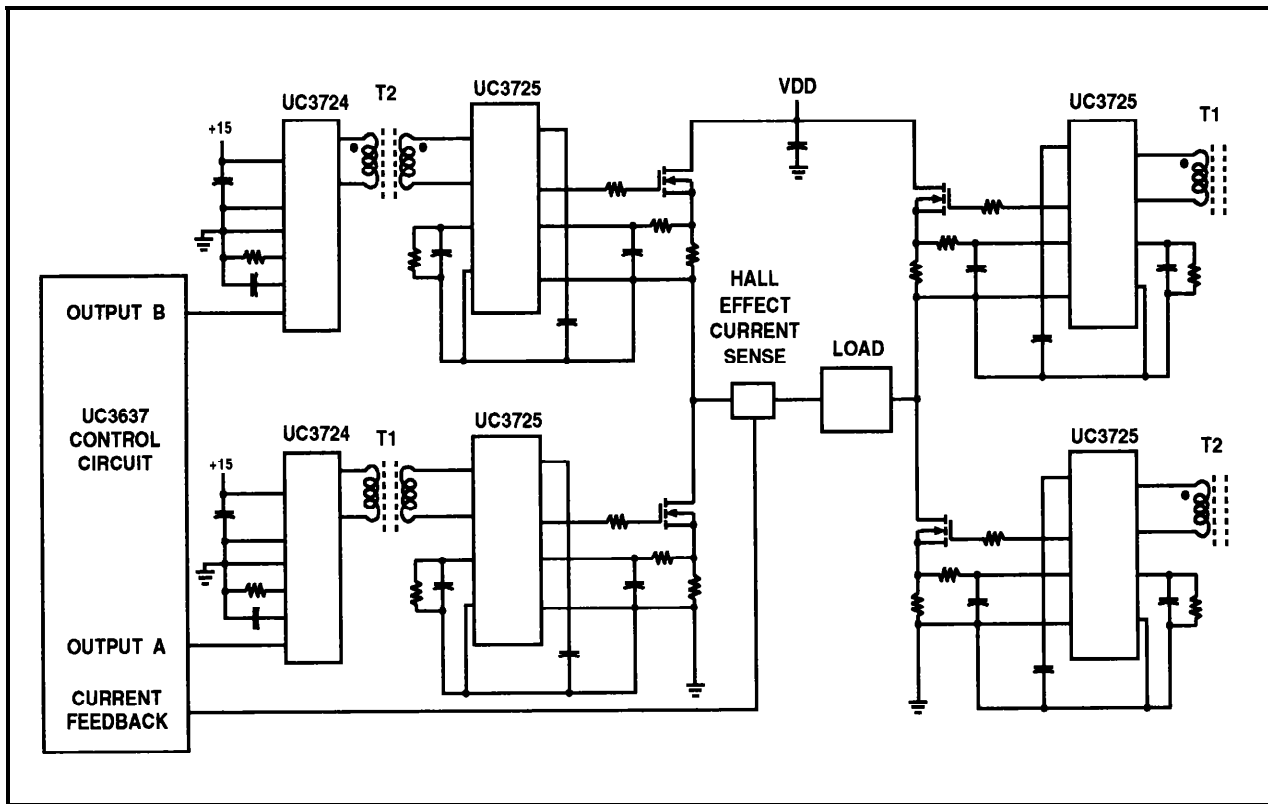


Figure 13

HALF BRIDGE OUTPUT CIRCUIT

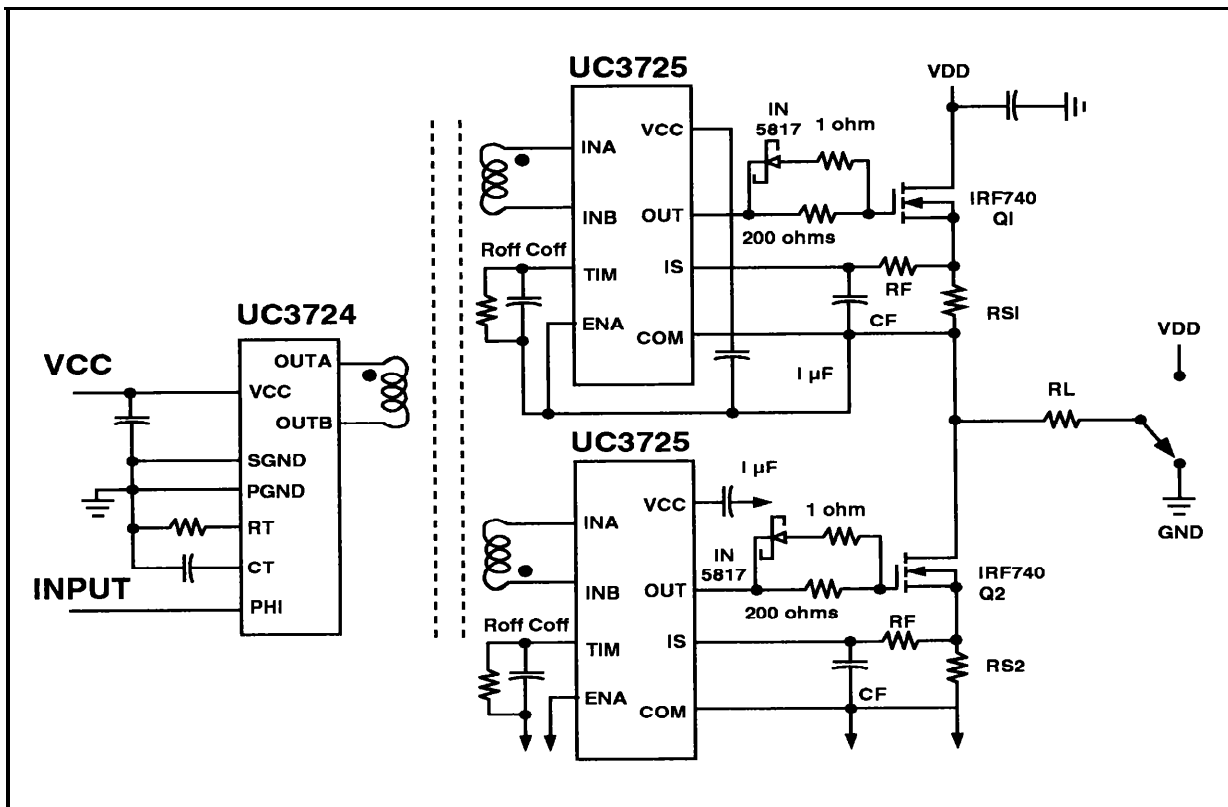


Figure 14

HALF BRIDGE OUTPUT

By reversing the polarity of one of the secondary windings on a dual secondary transformer, two FETs are switched out of phase from each other. A typical application for this arrangement is the half bridge, and is shown in figure 14. Dead-time between turn-off and turn-on is difficult to implement using this technique. To turn off both FETs, the UC3724 supply voltage must be removed, or the UC3725 enable inputs driven high. While shutting down the supply voltage is suitable for power-up/power-down protection, it is too slow to control dead-time. Isolating or level shifting the enable inputs adds complexity and negates the advantage of using a dual secondary transformer. Cross conduction is easily minimized however, by the gate resistor arrangement which provides rapid turn-off and slow turn-on. This technique is also typically used to minimize cross conduction caused by stored charge in the MOSFET body diode.

LEVEL SHIFT DRIVER

The UC3725 makes an excellent level shifted driver for lower voltage, non-isolated applications. All of the necessary protection features which are often omitted in discrete designs are incorporated in the UC3725 assuring reliable operation under all conditions. Figure 15 shows a typical level shift circuit with a "boot-strap" supply. The MPS-U10 level shift transistor has a maximum  $V_{ce0}$  of 300 volts, although its dissipation without a heatsink limits the maximum supply to approximately 200 volts. Figure 16 shows input to output propagation delay while switching 150 volts and 3 amps. A 20 mA current source with a voltage compliance 15 volts above the supply rail can be used in place of the boot-strap circuit, for applications which cannot tolerate an on-time limitation. The cost effectiveness of this approach will depend on supply voltage and number of high-side MOSFETs.

LEVEL SHIFT CIRCUIT

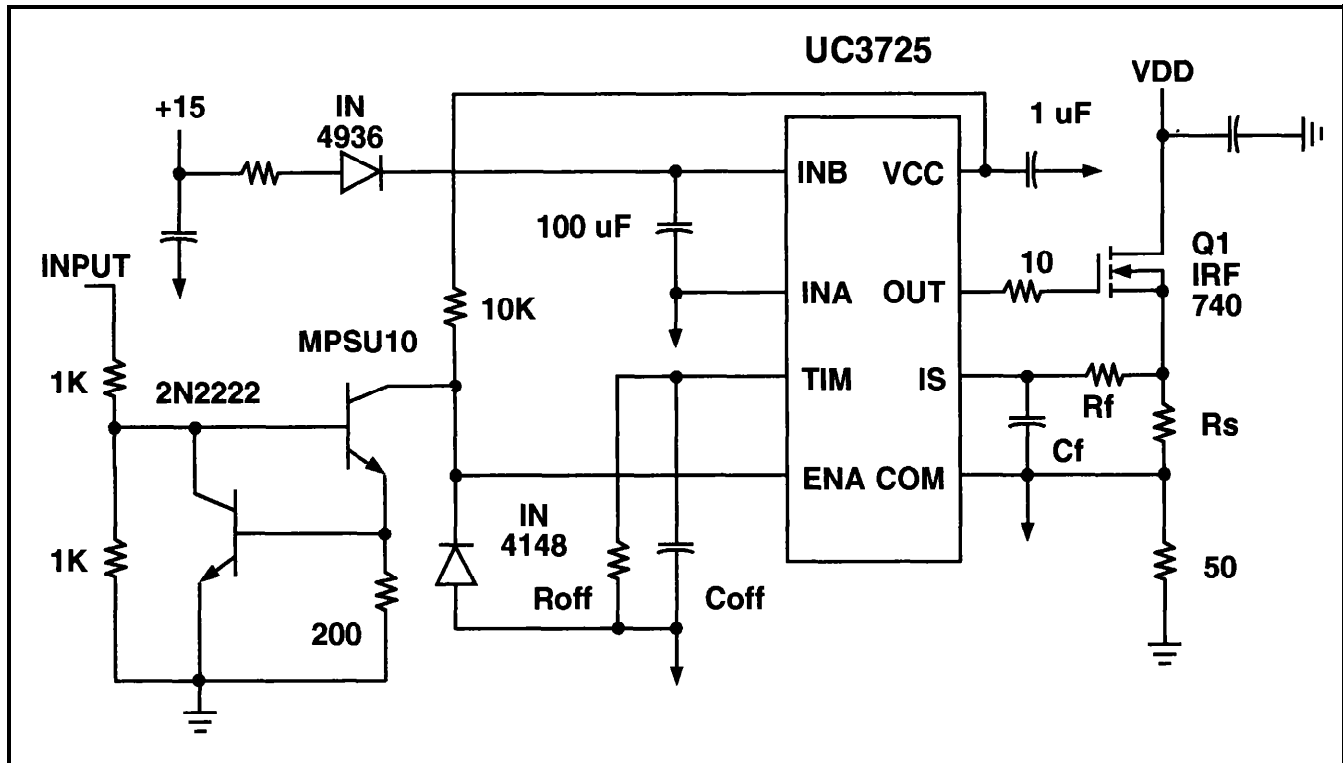


Figure 15

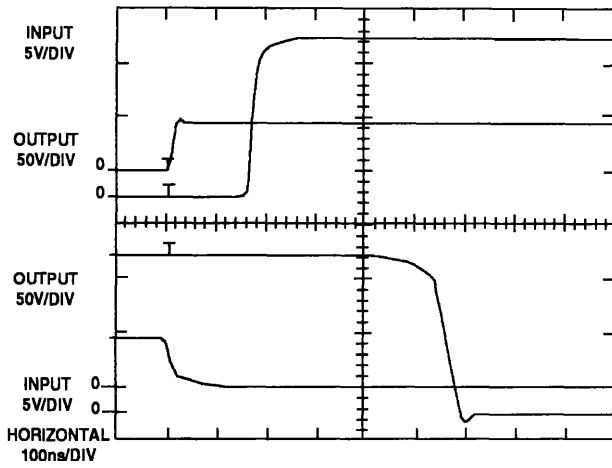


Figure 16.

**LATCHED OVER-CURRENT FAULT**

Current limiting is provided by the control circuit in many applications. Local protection from the UC3725 is therefore only required for fault conditions which result in high di/dt such as output shorts. It may be desirable to latch the output off under such a fault, rather than enable after a fixed off-time. Figure 17 shows a simple circuit used in place of the timing resistor and capacitor which

will latch the output off after the over-current comparator is triggered. The 10uF capacitor resets the circuit at power-up by holding the timing input below the 2 volt one-shot threshold. When an over-current is sensed, the timing input voltage falls, and is clamped at 5.1 volts. The one-shot period normally ends when  $C_{off}$  is discharged below 2 volts, but by clamping the voltage, the time constant effectively appears infinite.

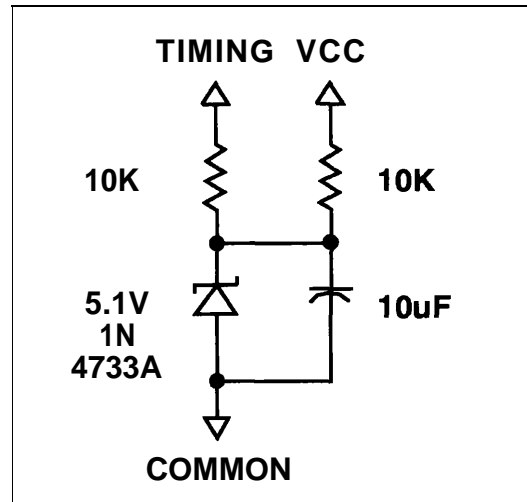


Figure 17

**FAST AC SWITCH**

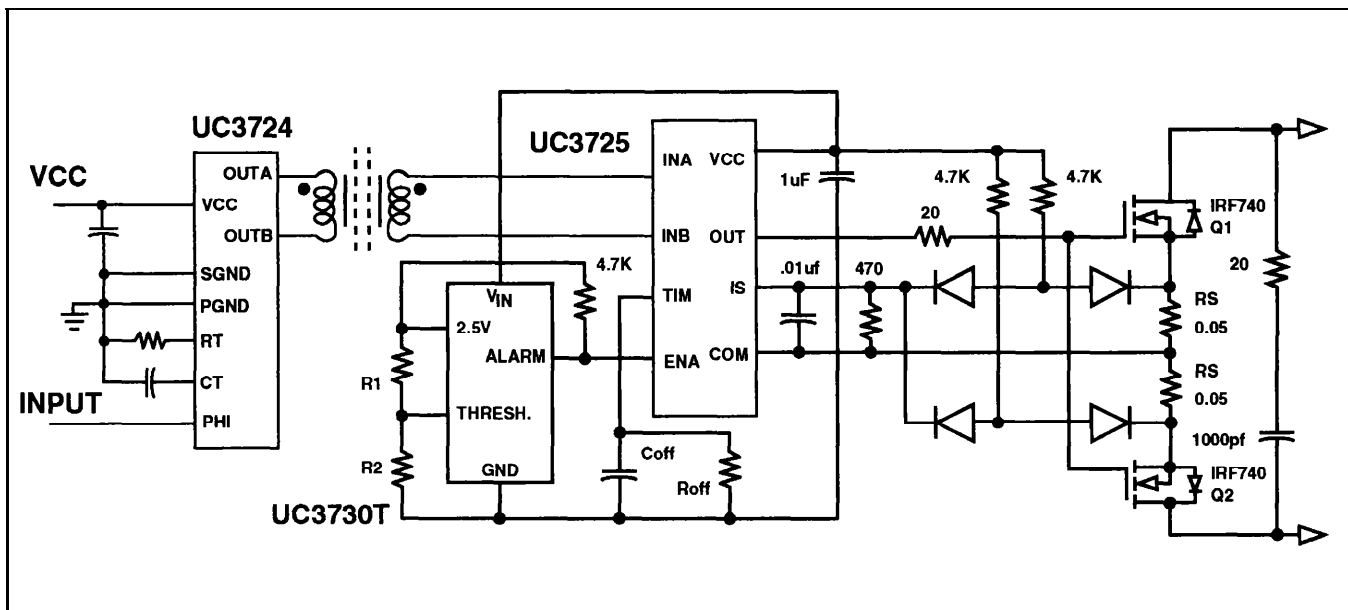


Figure 18

## FAST AC SWITCH

## SUMMARY

Fully isolated gate drive lends itself to unique power switching circuits which are otherwise extremely difficult to implement. Figure 18 is a fast AC switch with over-current and over-temperature protection. The MOSFETs are selected to withstand the peak AC voltage, with each FET blocking in the opposite polarity. Figure 19 shows a 100 ohm load switched across 115 VAC, 60 Hz. The diode network allows current sensing in both directions, with the 4.7K resistors functioning as current sources. Protection against excessive MOSFET junction temperature is accomplished by mounting both FETs and the UC3730T on the same heatsink. MOSFET thermal resistance (junction to heatsink), and maximum FET dissipation must be considered when selecting the shut-down temperature set by R1 and R2. Refer to UC3730 datasheet for additional information. A 1000pf/20 ohm snubber is connected across the switch to reduce turn-off voltage spiking. The actual snubber values required are determined by load conditions.

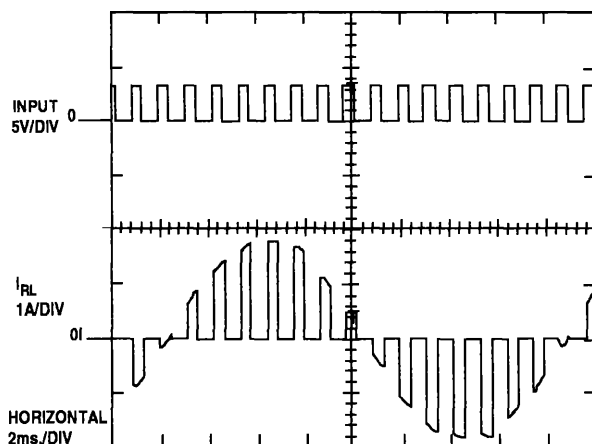


Figure 19.

A unique integrated circuit pair, the UC3724/UC3725 has been presented that provides a simple, low cost, isolated MOSFET gate drive solution. Protection features prevent abnormal gate drive voltage, and provide over-current limiting. Duty cycle or on time limitations typical of other techniques are avoided, and by utilizing a transformer for isolation, there are no inherent isolation voltage limitations. The circuit is suitable for fully isolated systems which must meet UL or VDE requirements, as well as typical high-side switch applications.

## REFERENCES

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2. W. Andreyckak, "1.5 MHz CURRENT MODE IC CONTROLLED 50 WATT POWER SUPPLY", UNITRODE APPLICATION NOTE # U-110
3. W. Andreyckak, "A NEW GENERATION OF HIGH PERFORMANCE MOSFET DRIVERS FEATURES HIGH CURRENT, HIGH SPEED OUTPUTS", UNITRODE APPLICATION NOTE # U-126